DOCUMENT NUMBER AND REVISION
VL-FS-MDLS16265SS3-03 REV. B
(MDLS16265SS-3V-C16)

DOCUMENT TITLE:
SPECIFICATION
OF
LCD MODULE TYPE
MODEL NUMBER: MDLS16265SS3-03

DEPARTMENT	NAME	SIGNATURE	DATE
PREPARED BY	HELEN HE	Helen He	2004.04.19
CHECKED BY	HE ZUO BING	He Zuobing	04.04.19
APPROVED BY	DERRICK TAM		2004.4.20

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VARITRONIX LIMITED

Specification
of
LCD Module Type
Item No.: MDLS16265SS3-03

1. General Description

- 16 characters (5x8 dots) x 2 lines STN Positive Reflective Yellow LCD Character Module.
- Viewing Angle: 6 O'clock direction.
- Driving duty: 1/16 Duty, 1/3 bias.
- 'SAMSUNG' KS0070BP-00CC (die form) LCD Controller & Driver or equivalent.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1(A) and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	84.0(W) x 44.0(H) x 10.0 MAX.(D)	mm
Effective viewing area	61.0(W) x 15.8(H)	mm
Display format	16 characters x 2 lines	-
Character size	2.95(W) x 5.55(H) (5 x 8 dots)	mm
Character spacing	0.60(W) x 0.40(H)	mm
Character pitch	3.55(W) x 5.95(H)	mm
Dot size	0.55(W) x 0.65(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.60(W) x 0.70(H)	mm
Weight:	TBD	grams

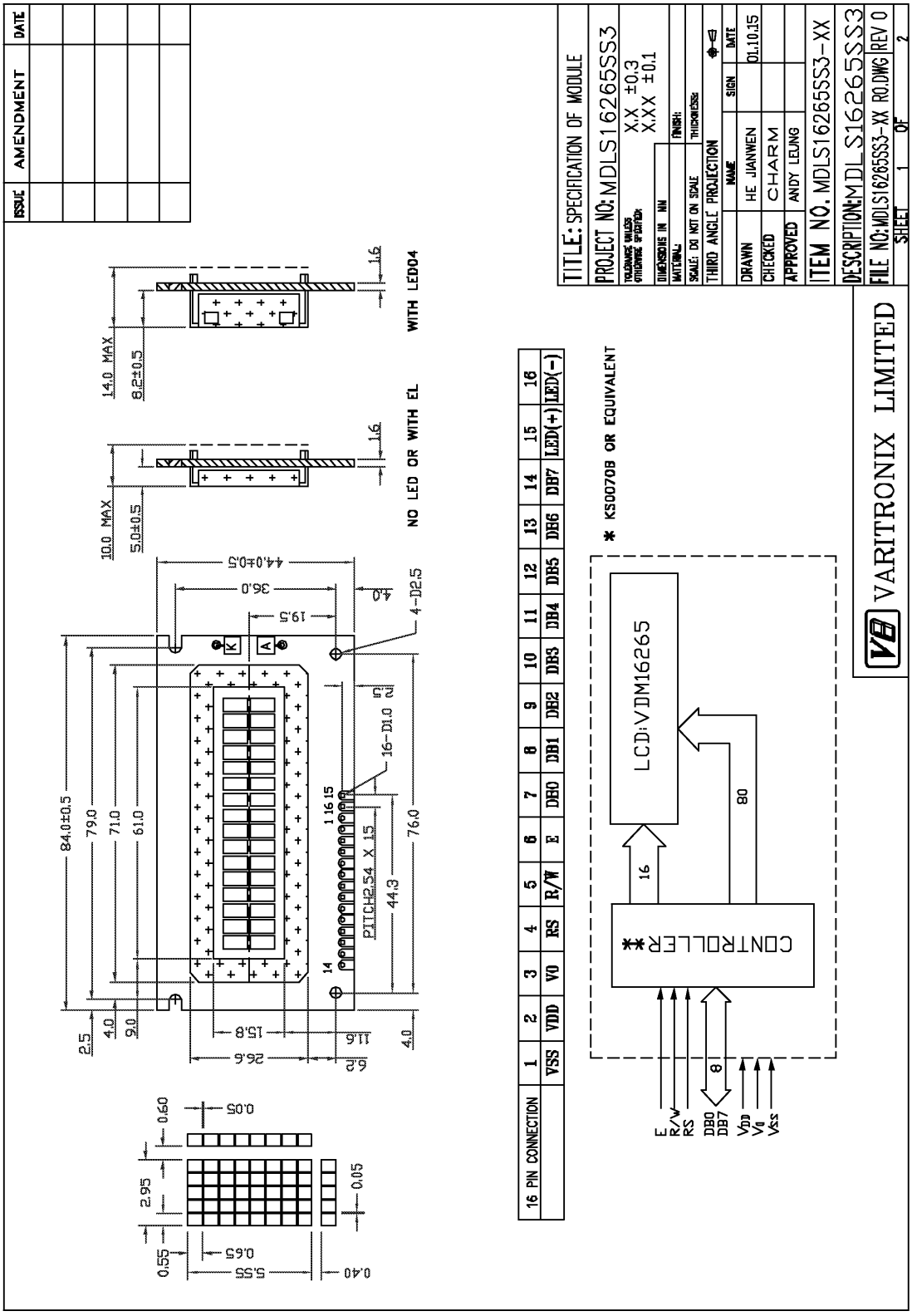


Figure 1(A): Outline Drawing 1

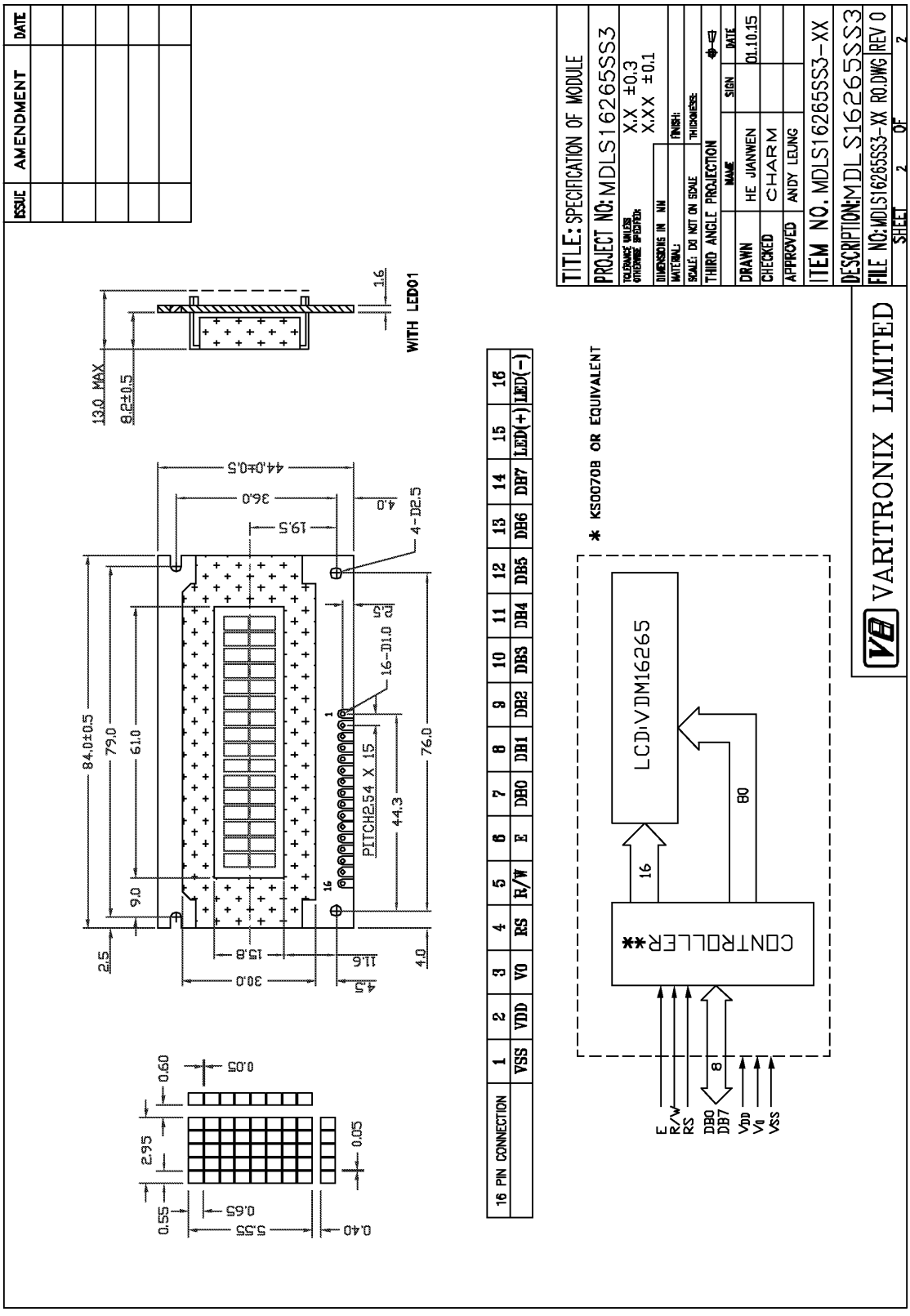


Figure 1(B): Outline Drawing 2

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic(+3V).
3	V0	Power supply for LCD driver.
4	RS	Register Select Input: 'High' for Data register (for read and write). 'Low' for Instruction register (for write), Busy flag, address counter (for read).
5	R/W	Read/Write signal: 'High' for Read mode. 'Low' for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB).
8	DB1	Data input/output.
9	DB2	Data input/output.
10	DB3	Data input/output.
11	DB4	Data input/output.
12	DB5	Data input/output.
13	DB6	Data input/output.
14	DB7	Data input/output (MSB).
15	LED(+)	Anode of LED Backlight (OPTIONAL).
16	LED(-)	Cathode of LED Backlight (OPTIONAL).

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD-VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD-V0	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-10°C	+55°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5% or 3.3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD -VSS		2.85	3.0	3.15	V
			3.13	3.3	3.46	V
Supply voltage (LCD)	VLCD =VDD –V0	VDD = 5V, Note (1)	2.8	3.0	3.2	V
Input signal voltage for E,DB0-DB7,R/W,RS.	V_{IH}	”H” level	0.7VDD	-	VDD	V
	V_{IL}	” L” level	-0.3	-	0.4	V
Supply Current (Logic & LCD)	IDD	Character mode, VDD=3V, Note (1)	-	0.8	1.2	mA
		Checker board mode, VDD=3V, Note (1)	-	1.3	2.0	mA
Supply Current (LCD)	I0	Character mode, VDD=3V, Note (1)	-	0.2	0.3	mA
		Checker board mode, VDD=3V, Note (1)	-	0.2	0.3	mA

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta = -10 °C To +55 °C , VDD = +3V±5% or 3.3V±5%, VSS = 0V.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	t_C	1400	-	ns	E
E rise time	t_r	-	25	ns	E
E fall time	t_f	-	25	ns	E
E pulse width (High, Low)	t_W	400	-	ns	E
R/W and RS set-up time	t_{SU1}	60	-	ns	R/W,RS
R/W and RS hold time	t_{h1}	20	-	ns	R/W, RS
Data set-up time	t_{SU2}	140	-	ns	DB0-DB7
Data hold time	t_{h2}	10	-	ns	DB0-DB7

Refer to Fig. 3, the bus timing diagram for read mode.

Table 7

Parameter	Symbol	Min.	Max.	Unit	Test pin
E cycle time	t_C	1400	-	ns	E
E rise time	t_r	-	25	ns	E
E fall time	t_f	-	25	ns	E
E pulse width (High, Low)	t_W	400	-	ns	E
R/W and RS set-up time	t_{SU}	60	-	ns	R/W,RS
R/W and RS hold time	t_h	20	-	ns	R/W, RS
Data output delay time	t_D	-	360	ns	DB0-DB7
Data hold time	t_{DH}	5	-	ns	DB0-DB7

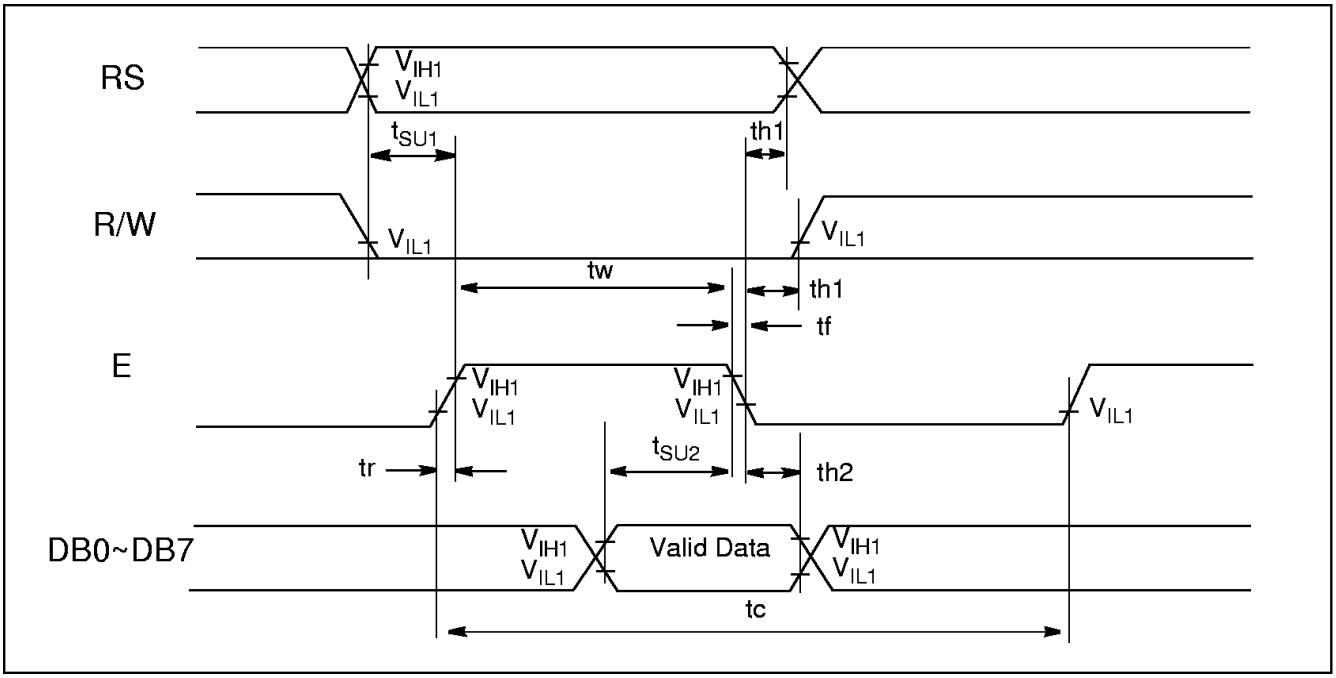


Figure 2: The bus timing diagram for write mode.

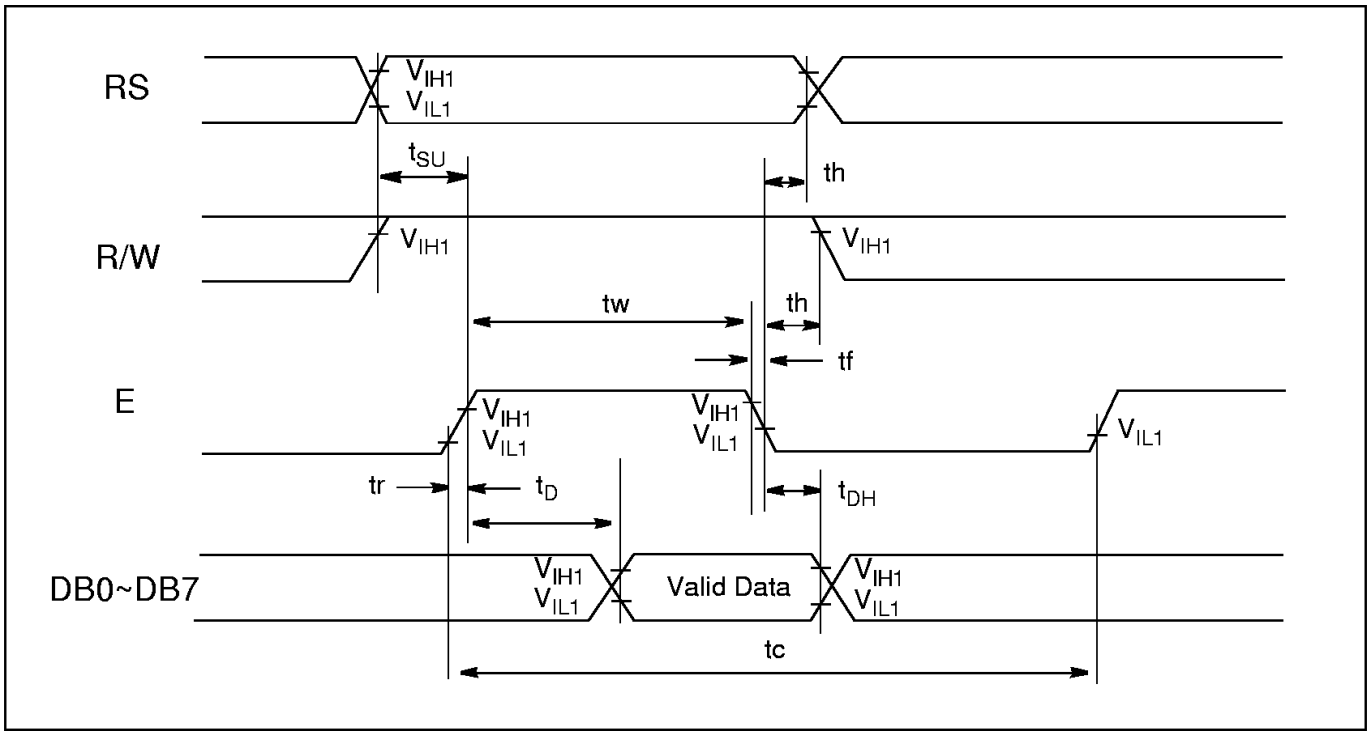


Figure 3: The bus timing diagram for read mode.

5.3 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

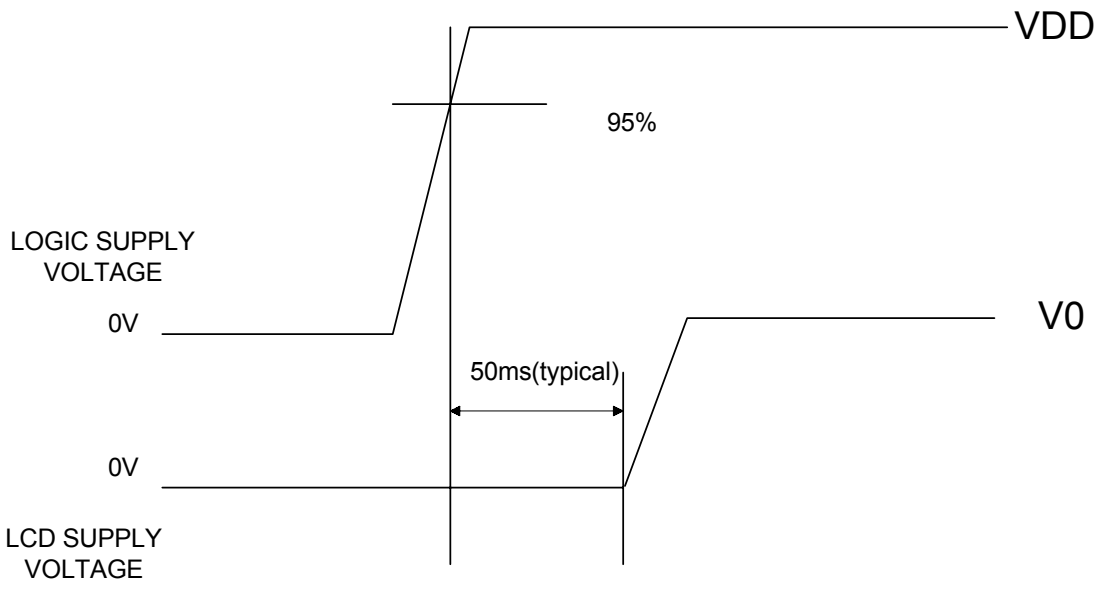
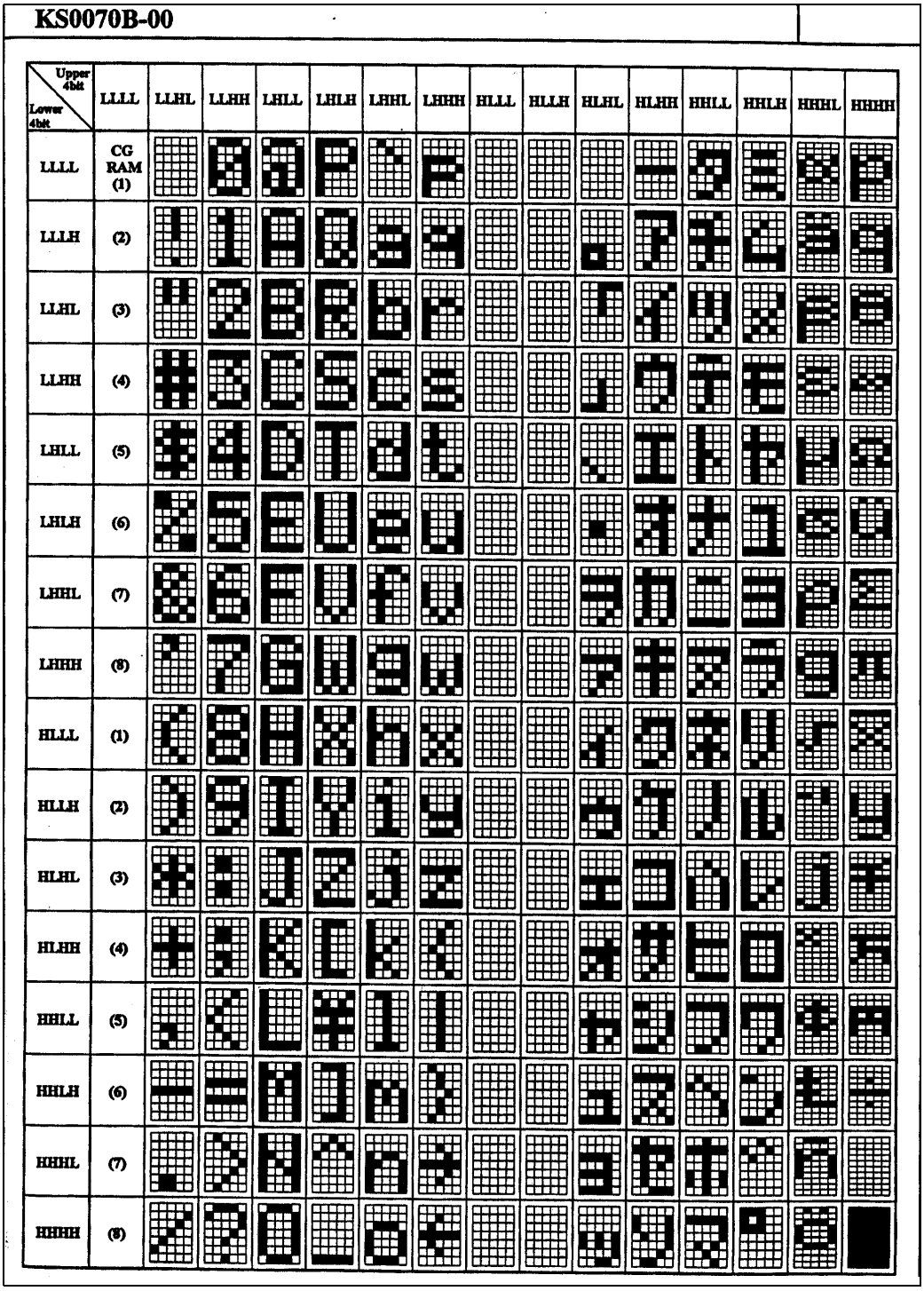


Figure 4: Timing Diagram of VDD Against V0.

6. CGROM Character Code Table

KS0070B-00



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FAX:(852) 2343-9555.

URL:http://www.varitronix.com

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